July 24th, 2013
Exam of Switching architectures

Rules for the exam. It is forbidden to use notes, books or calculators. When needed, use approximations.
Time available: 70 minutes.

PROBLEM A.
Design a rearrangeable switch of size $4096 \times 4096$ using only modules of size $8 \times 8$, with the aim of minimizing the number of modules.

1. What is the theoretical minimum number of modules needed? For the sake of easy computation, use the following approximation: $N! \approx \sqrt{N}N^N$.
2. Describe the proposed architecture
3. Compute the total number of modules required and compare it with the minimum one obtained in question 1.
4. Describe how to configure the overall network

PROBLEM B.
Consider a generic frame scheduling policy for input queued switches in which the arrival rates are known and the scheduling decision are taken oblivious of the queue state.

1. Prove that the average delay grows as $O(N)$ in order sense, for one of the possible frame scheduling algorithms.
2. Is it possible to improve the average delay in order sense? How?

If needed, for a slotted Geom/Geom/1 queue with arrival probability $\lambda$ and service probability $\mu$, the average delay is:

$$W_{Geom/Geom/1} = \frac{\eta}{\lambda(1-\eta)} \quad \text{with} \quad \eta = \frac{\lambda(1-\mu)}{\mu(1-\lambda)}$$

If needed, for a slotted M/D/1 queue with binomial $(N, \rho/N)$ arrivals per slot, the average delay is:

$$W_{M/D/1} = 1 + \frac{\rho}{2(1-\rho)}$$

PROBLEM C.
Consider a $N \times N$ input queued switch with just one single FIFO queue per each input, fed by admissible Bernoulli i.i.d. arrivals.

1. Explain in details the meaning of admissible Bernoulli i.i.d. arrivals.
2. Describe the performance in terms of average delay and throughput, under uniform traffic. Draw the corresponding two performance curves: throughput vs load, delay vs load.
3. Describe a non-uniform traffic scenario in which the throughput is always maximum. Draw the two performance curves, as above.
4. Describe a non-uniform traffic scenario in which the throughput is very small. Draw the two performance curves, as above.
HINTS FOR THE SOLUTIONS

Problem A
See exercise 8 and problem B of 11/02/2013.

\[ C_{4096} = 1024C_8 + 8C_{512} = 3584C_8 \]
\[ C_{512} = 128C_8 + 8C_{64} = 320C_8 \]
\[ C_{64} = 24C_8 \]

The minimum number of modules \( \hat{C} \) can be computed:

\[ \hat{C} = \frac{\log_2(4096!)}{\log_2(8!)} C_8 \]

Given the approximation:

\[ \log_2(N!) = N \log_2 N + 0.5 \log_2 N \]

By simple computations (by hand):

\[ \log_2(4096!) = 49158 \quad \log_2(8!) = 25.5 \]

and finally:

\[ \hat{C} \approx \frac{50000}{25} = 2000C_8 \]

Hence, the devised architecture has less than twice the number of modules than the minimum one.

Problem B
See problem C of 31/01/2012. See slides on the “Scalability of delays in input queued switches”.

Problem C
See class notes.